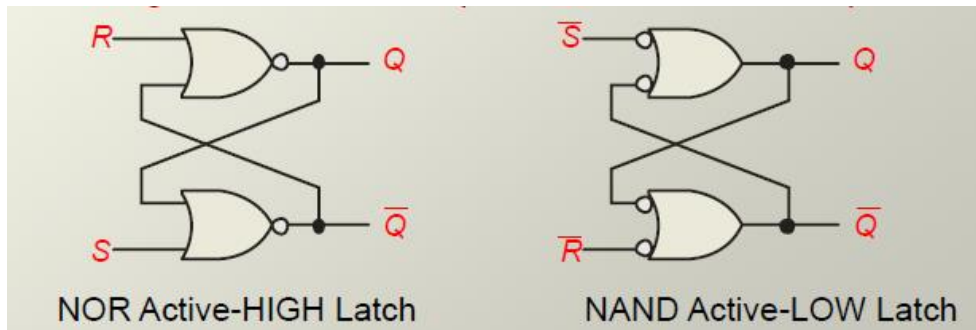


## Latches and Flip Flops Lab in Proteus

The S-R (Set-Reset) latch is the most basic type. It can be constructed from NOR gates or NAND gates.

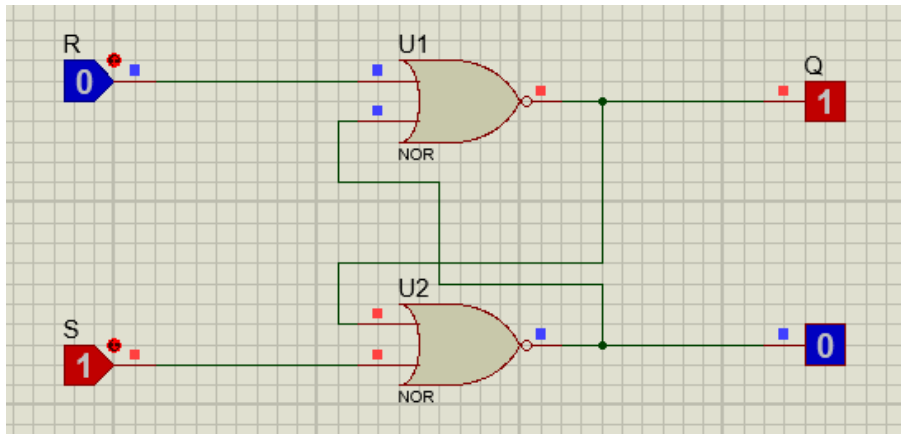
- With NOR gates, the latch responds to active-HIGH inputs.
- With NAND gates, the latch responds to active-LOW inputs.



### Active High Latch in Proteus

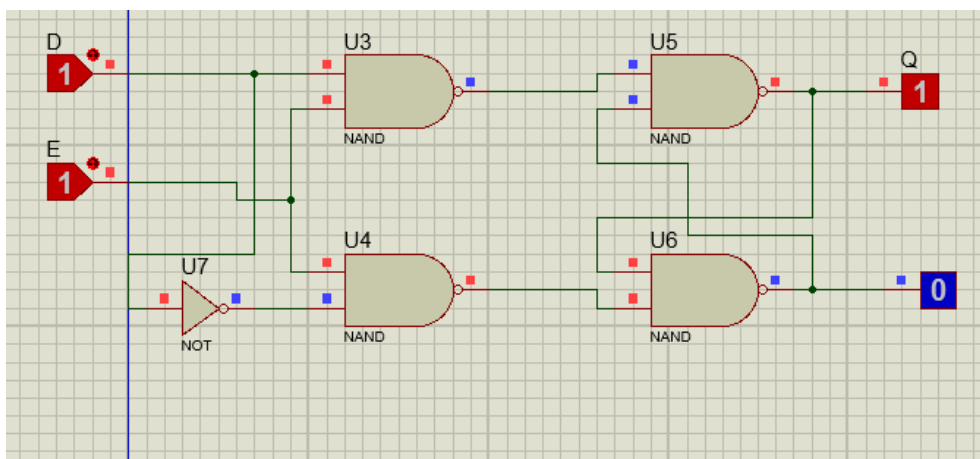
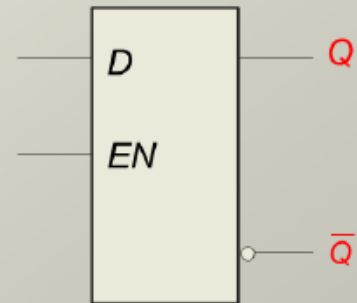
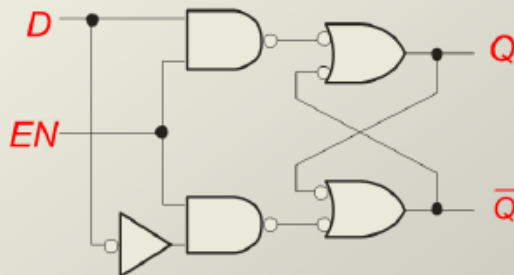
The image shows a comparison between a logic gate implementation and a Proteus component block. On the left is the NOR-based implementation with inputs R and S, and outputs Q and Q-bar. On the right is a Proteus component block with inputs R and S, and outputs Q and Q-bar.

INPUTS		OUTPUTS		COMMENTS
S	R	Q	Q̄	
0	0	NC	NC	No change. Latch remains in present state.
0	1	0	1	Latch RESET.
1	0	1	0	Latch SET.
1	1	0	0	Invalid condition



Gated D Latch in Proteus

Inputs		Outputs		Comments
D	EN	Q	$\bar{Q}$	
0	1	0	1	RESET
1	1	1	0	SET
X	0	$Q_0$	$\bar{Q}_0$	No change



## J-K flip-flop in proteus( ic number 74111)

Inputs			Outputs		Comments
J	K	CLK	Q	$\bar{Q}$	
0	0	↑	$Q_0$	$\bar{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\bar{Q}_0$	$Q_0$	Toggle

